

FIG. I (PRIOR ART)

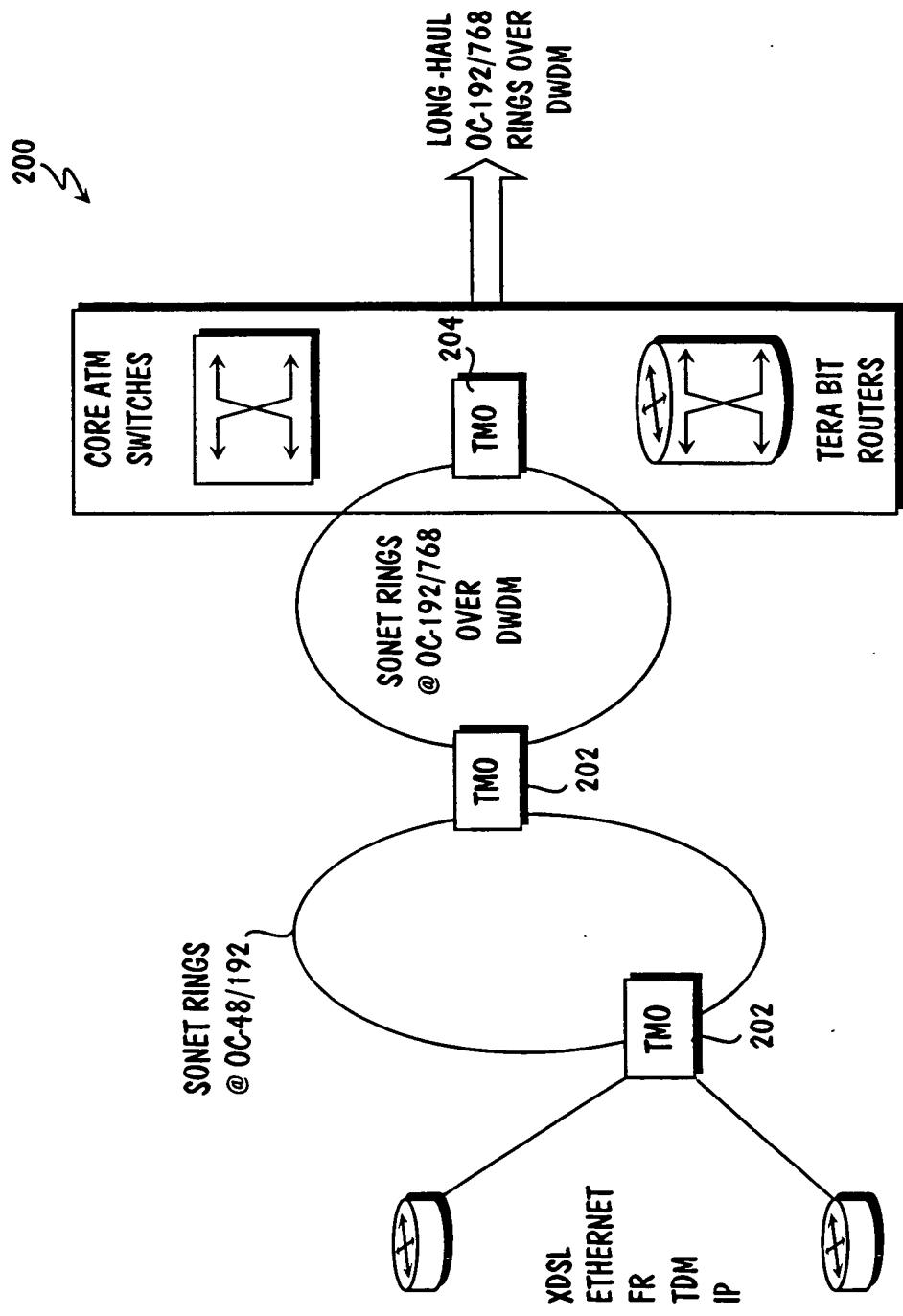


FIG. 2

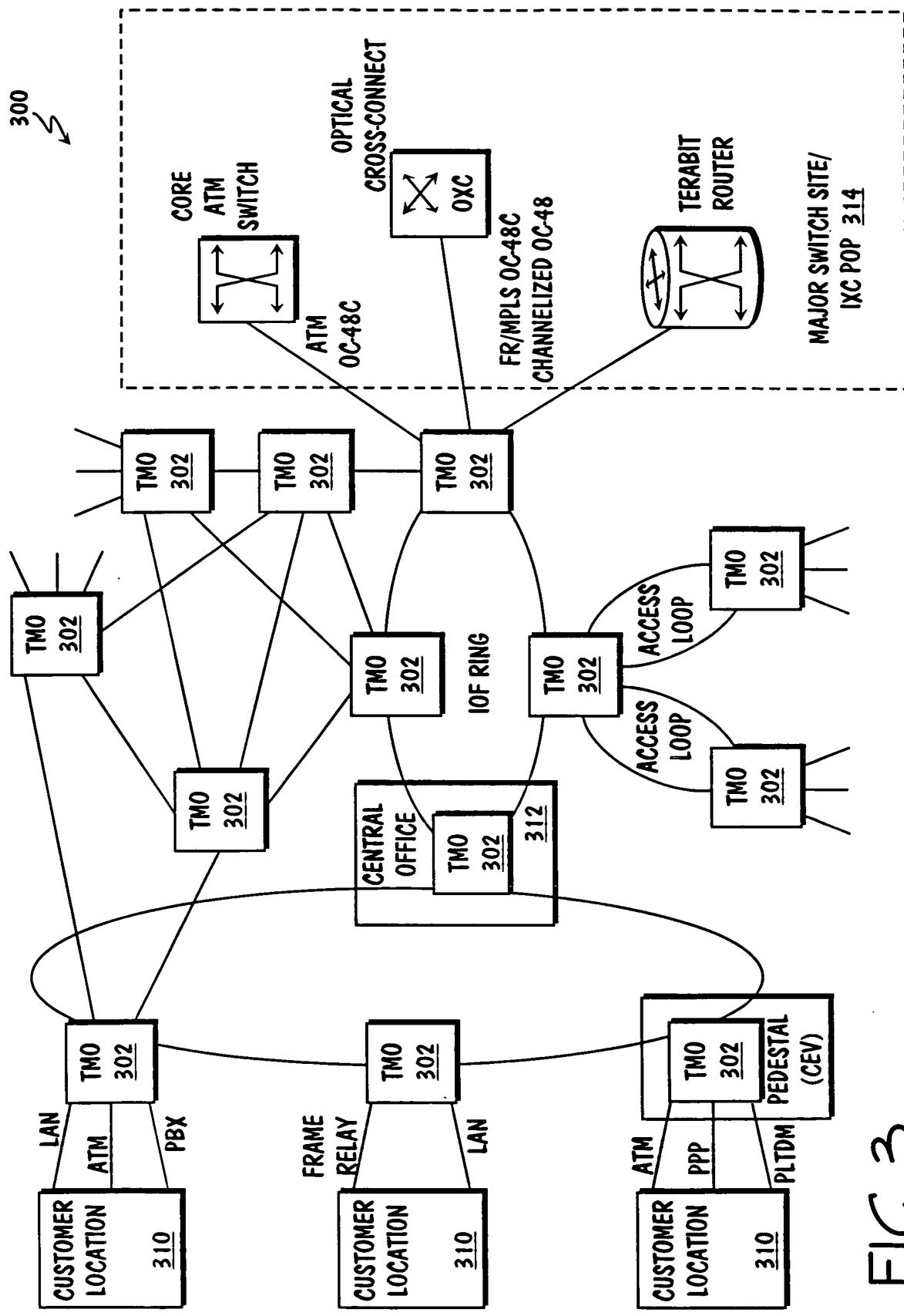
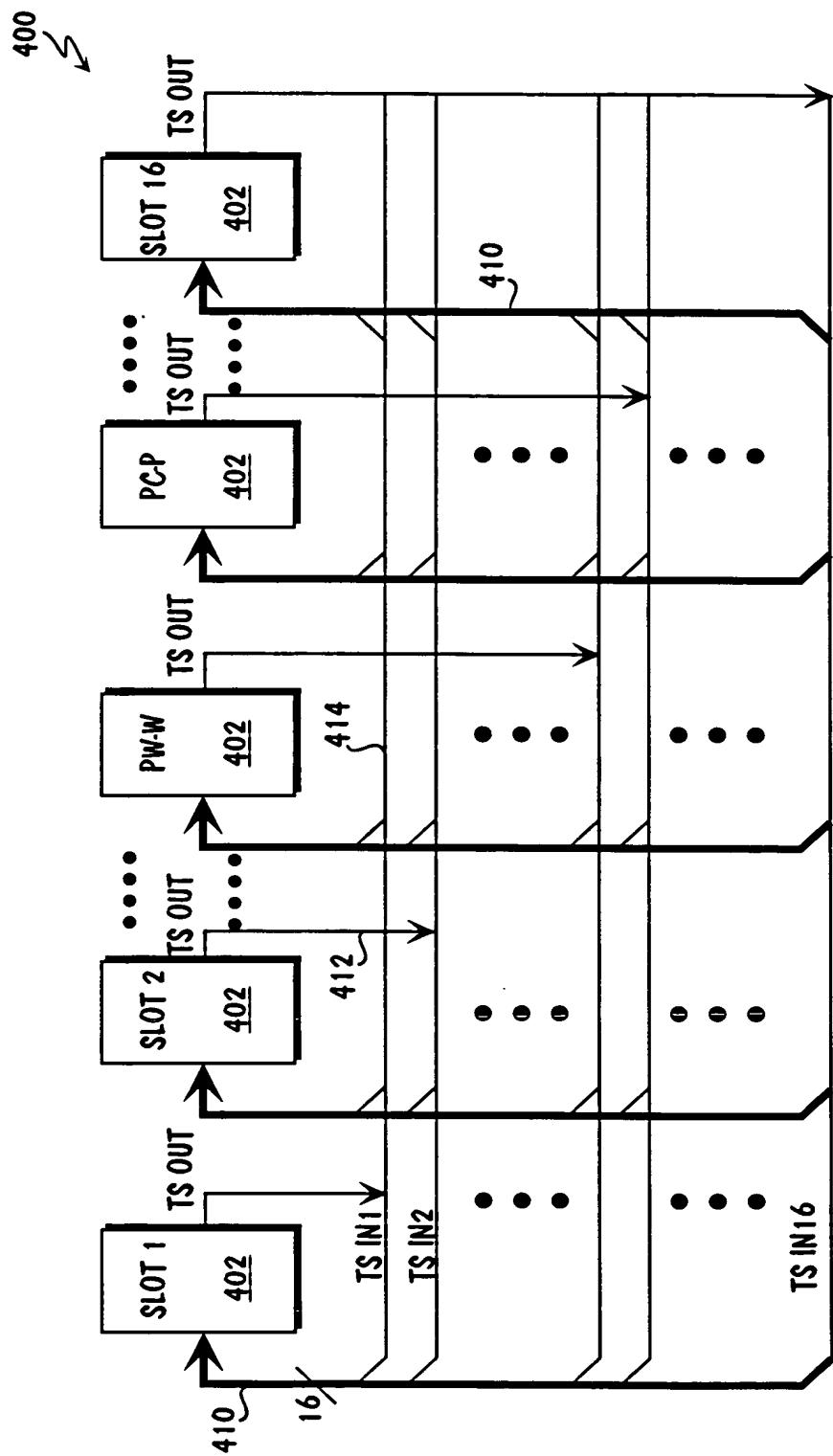


FIG. 3



4
Fig.

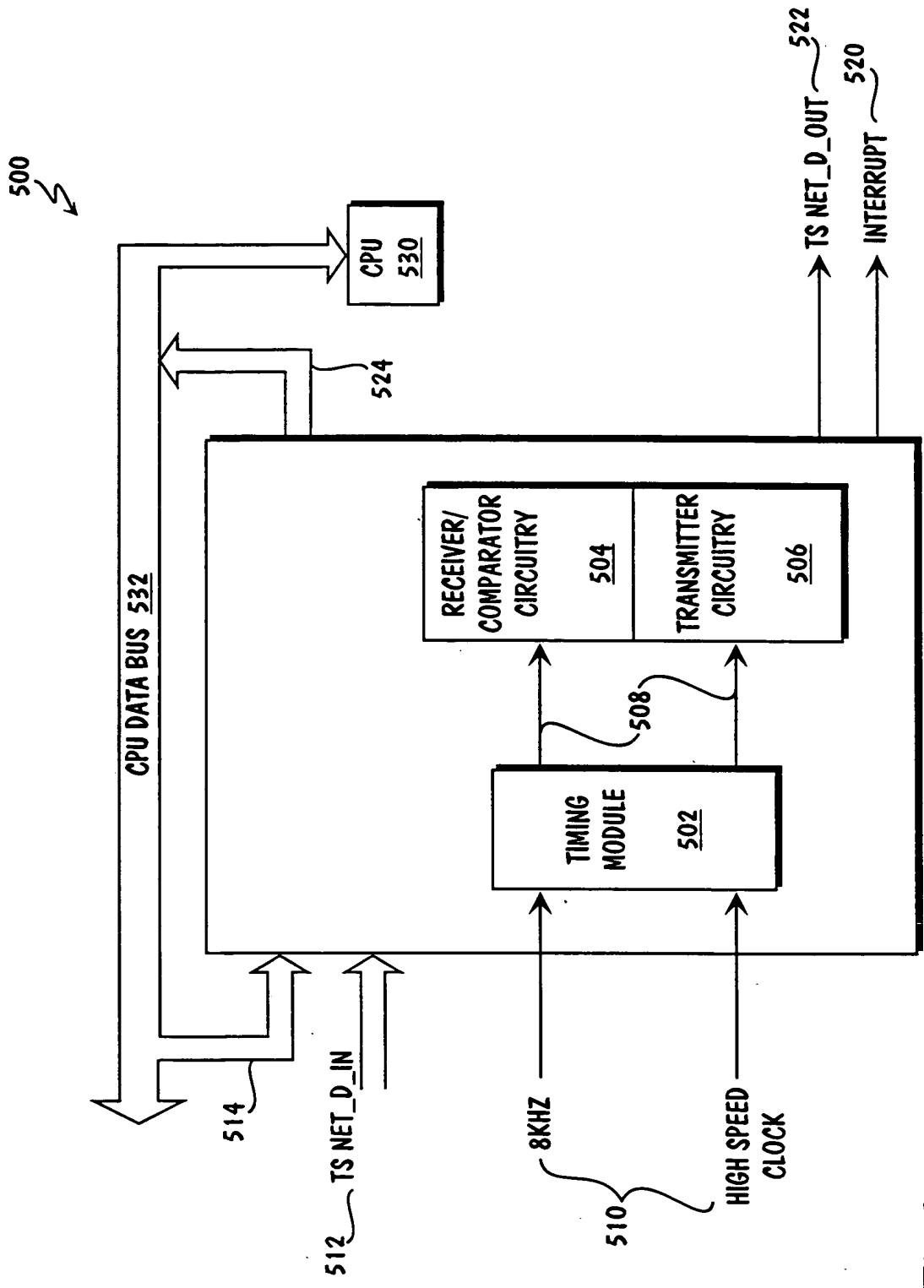


FIG. 5

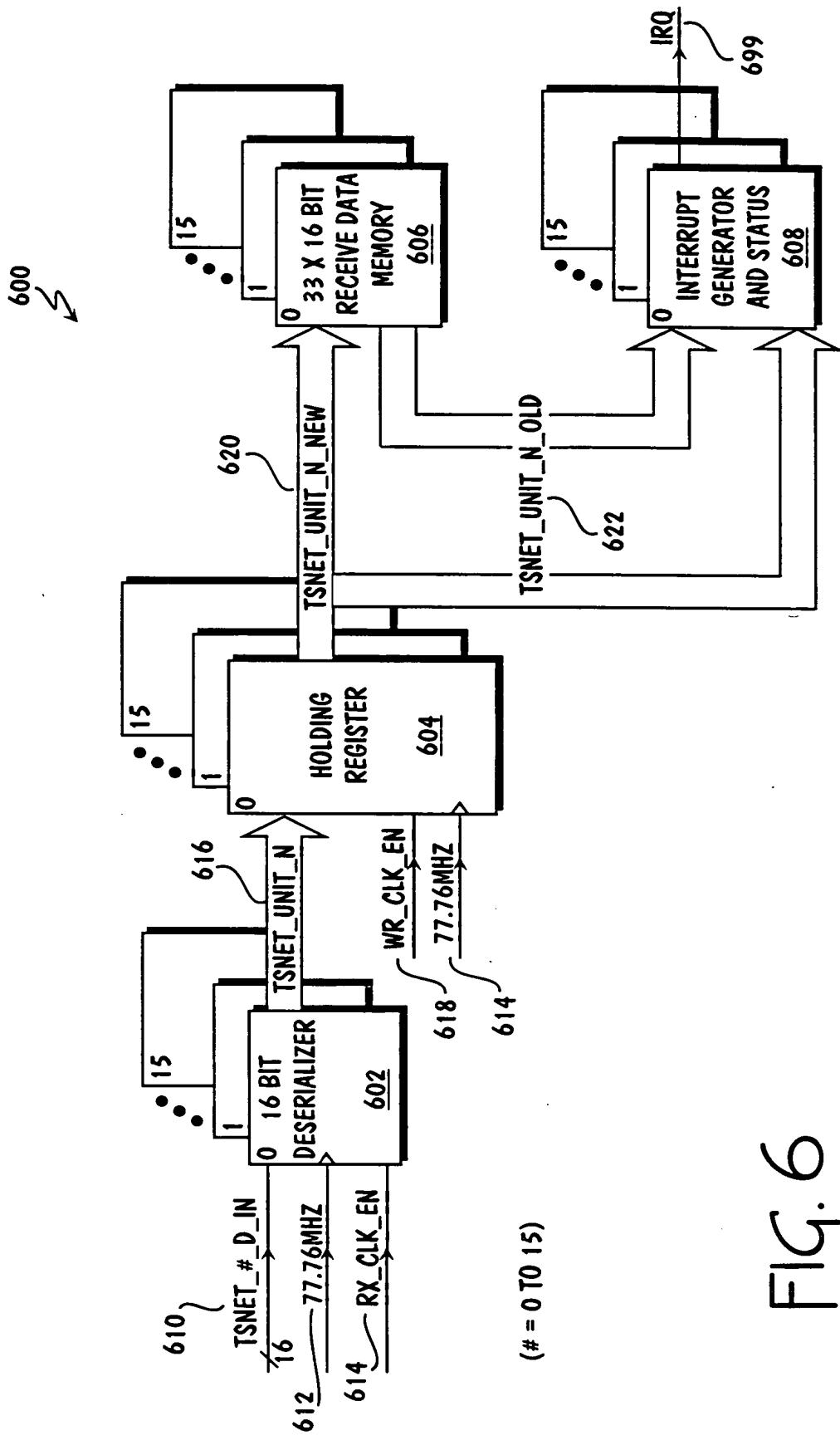


FIG. 6

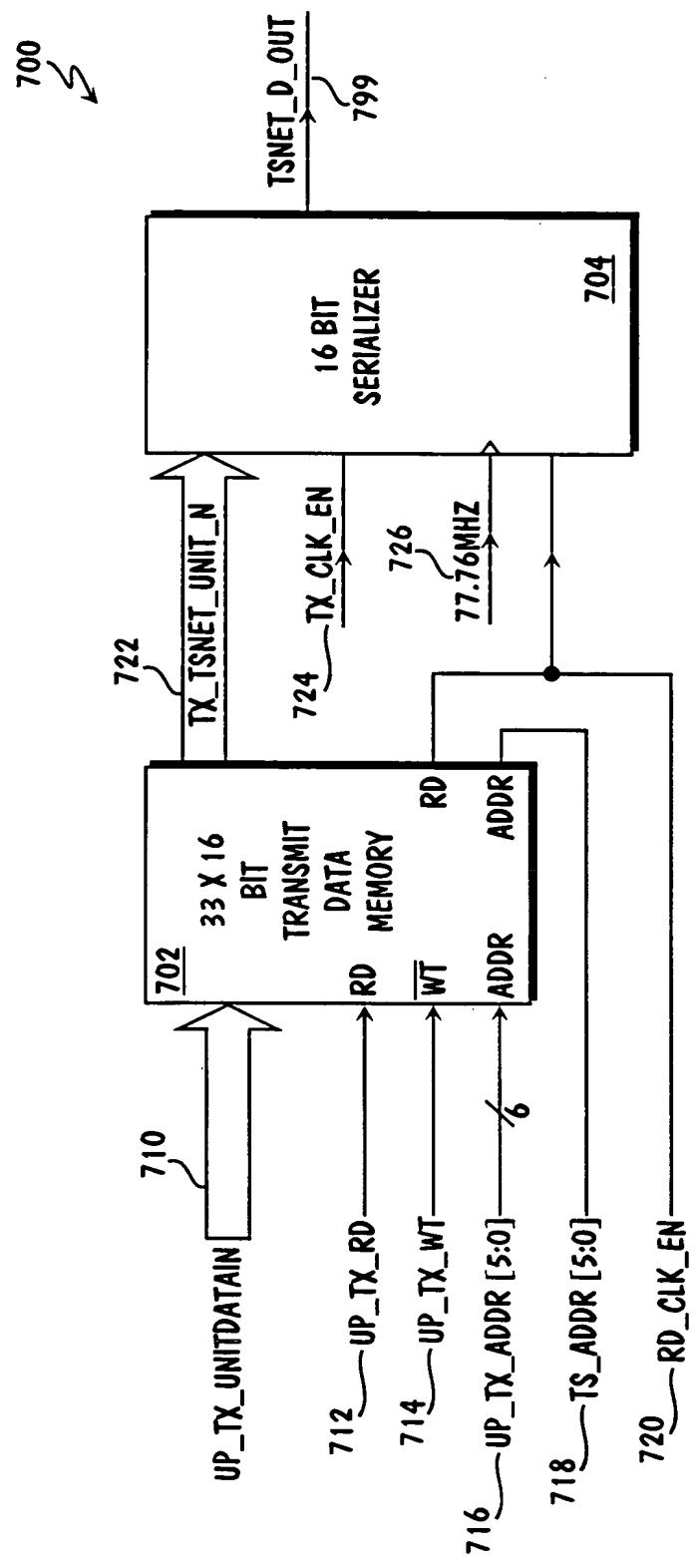


FIG. 7

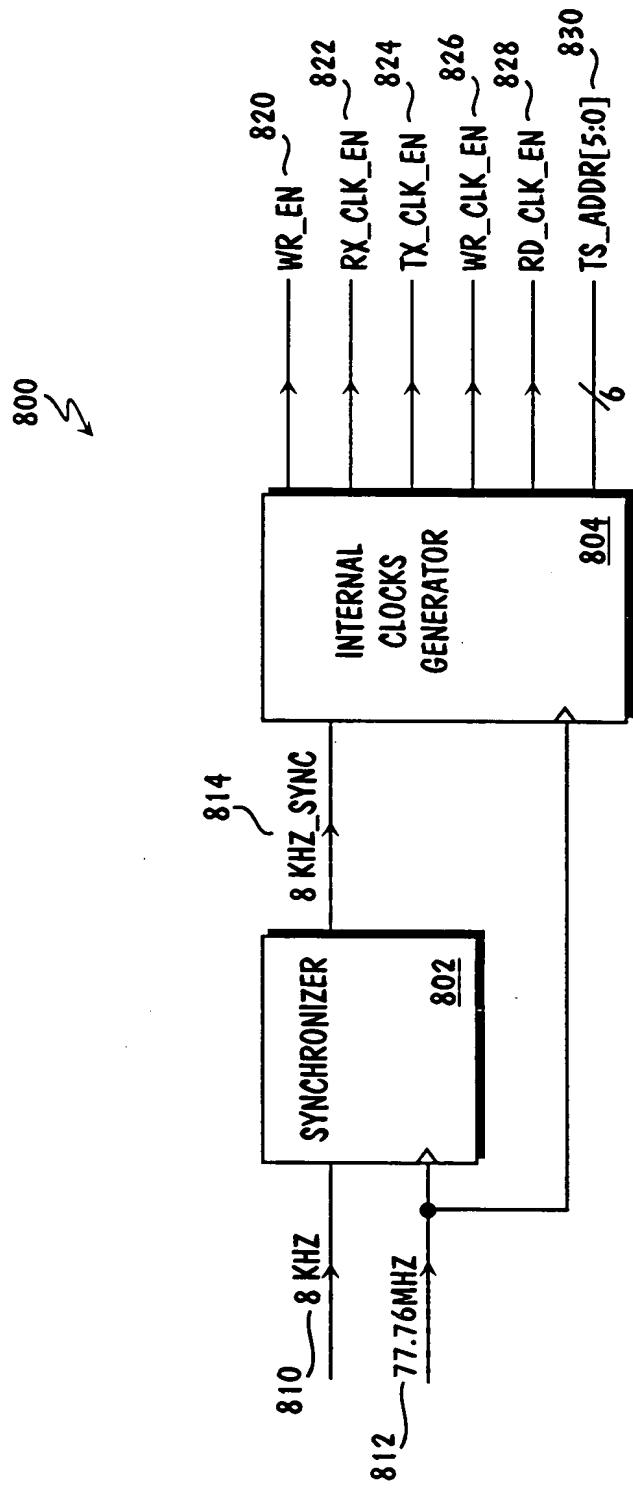
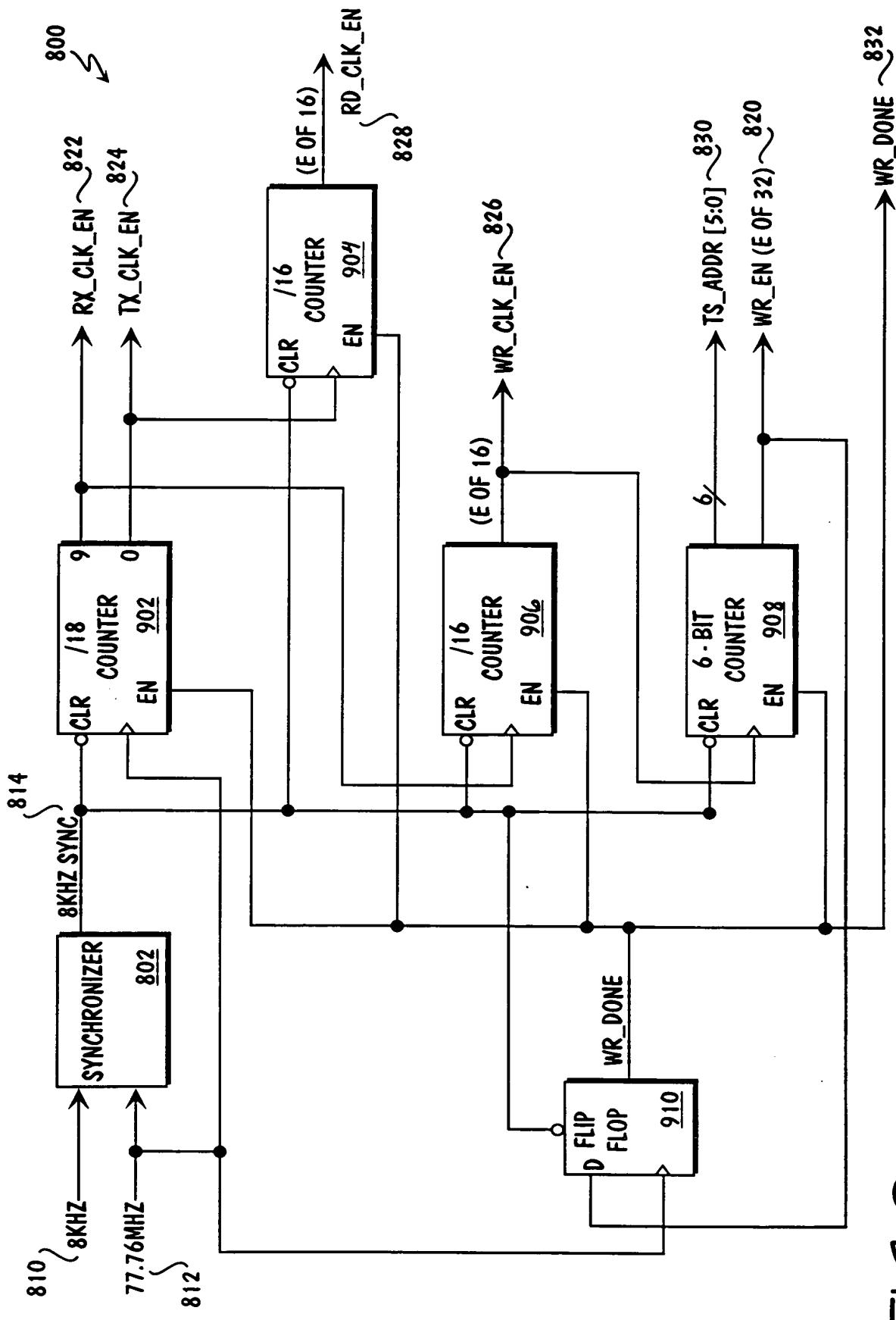


FIG. 8



6
二
正

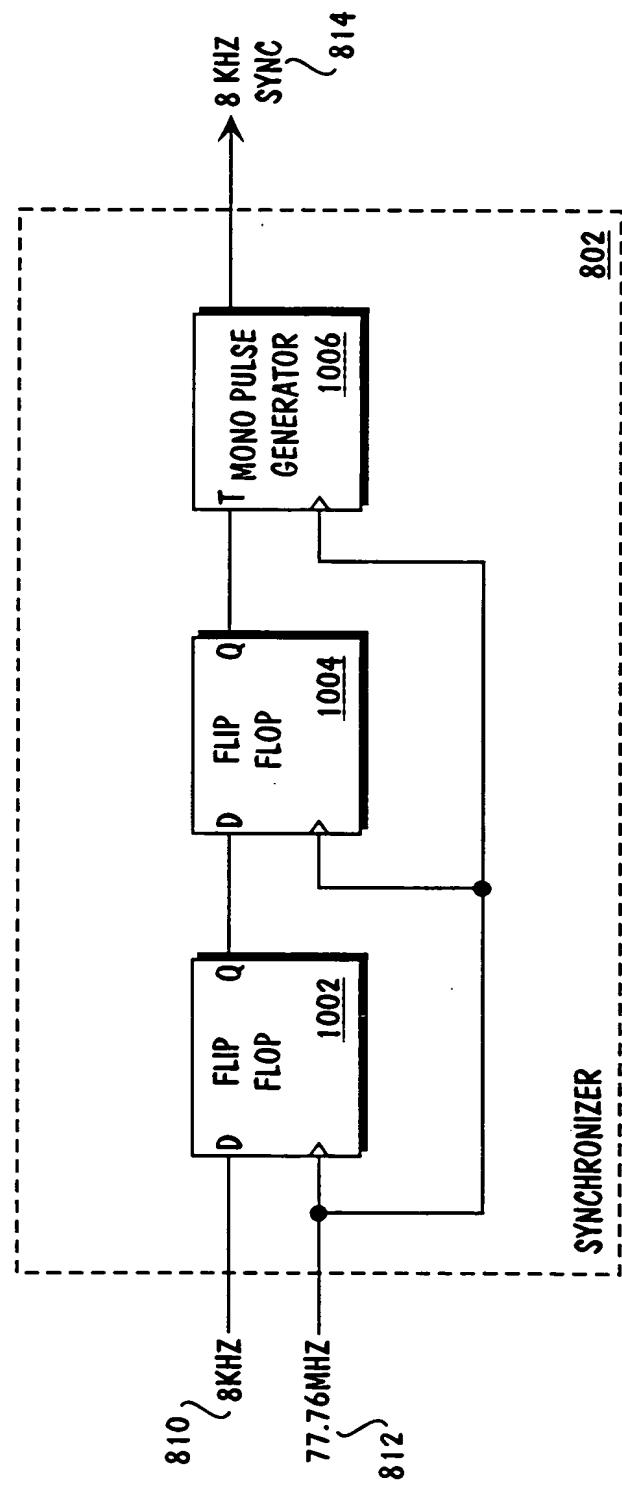


FIG. 10

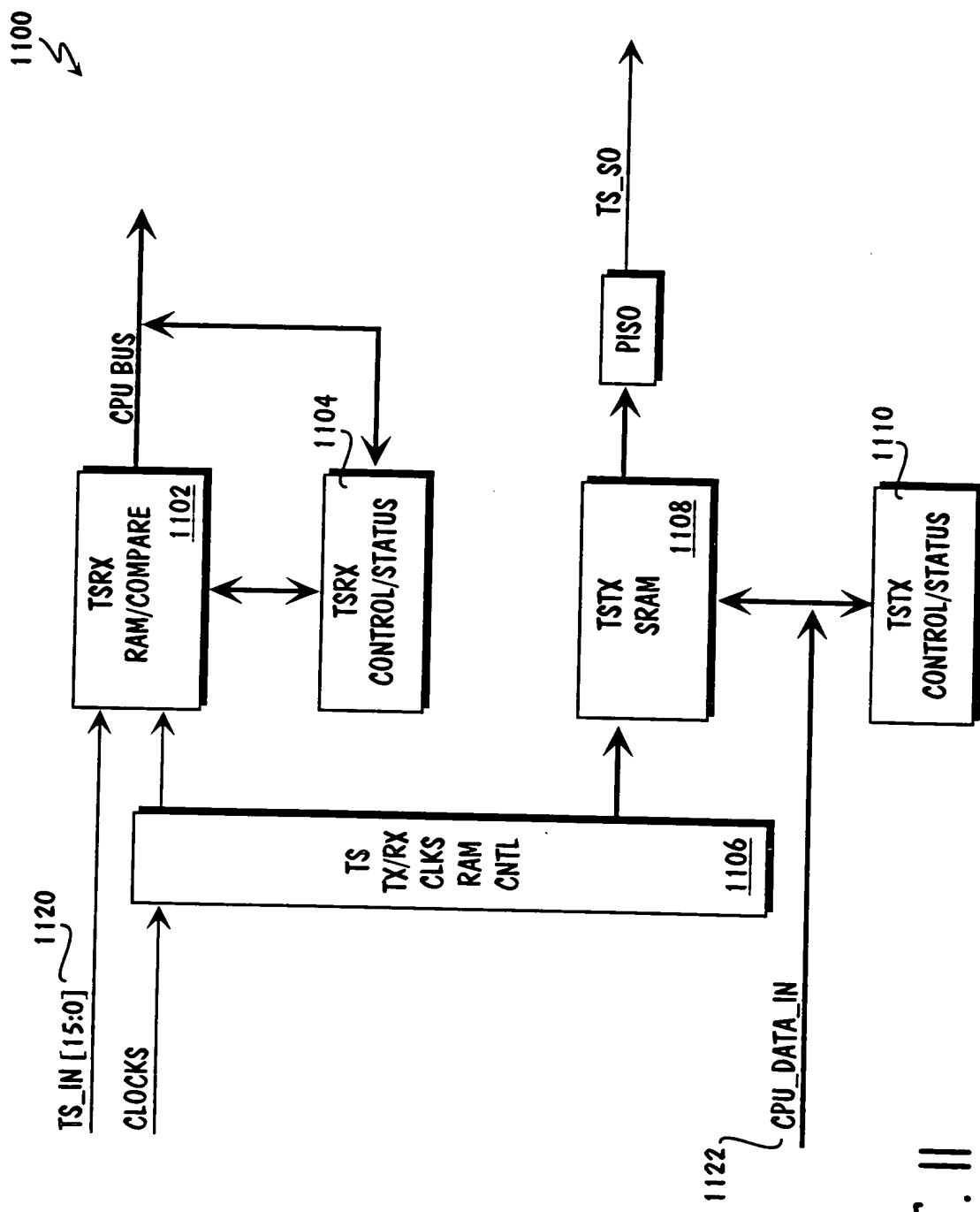
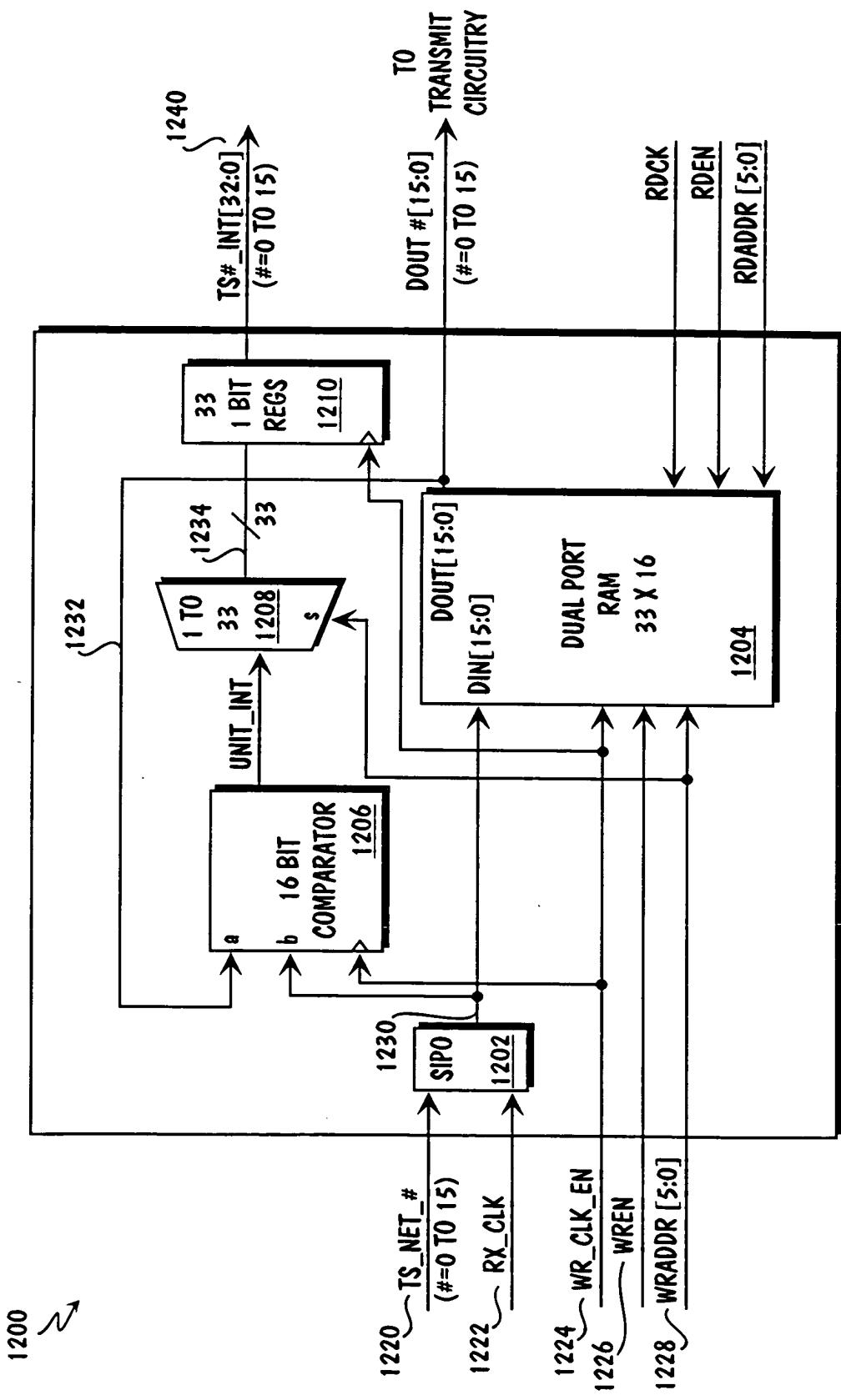


FIG. II

Fig. 12A



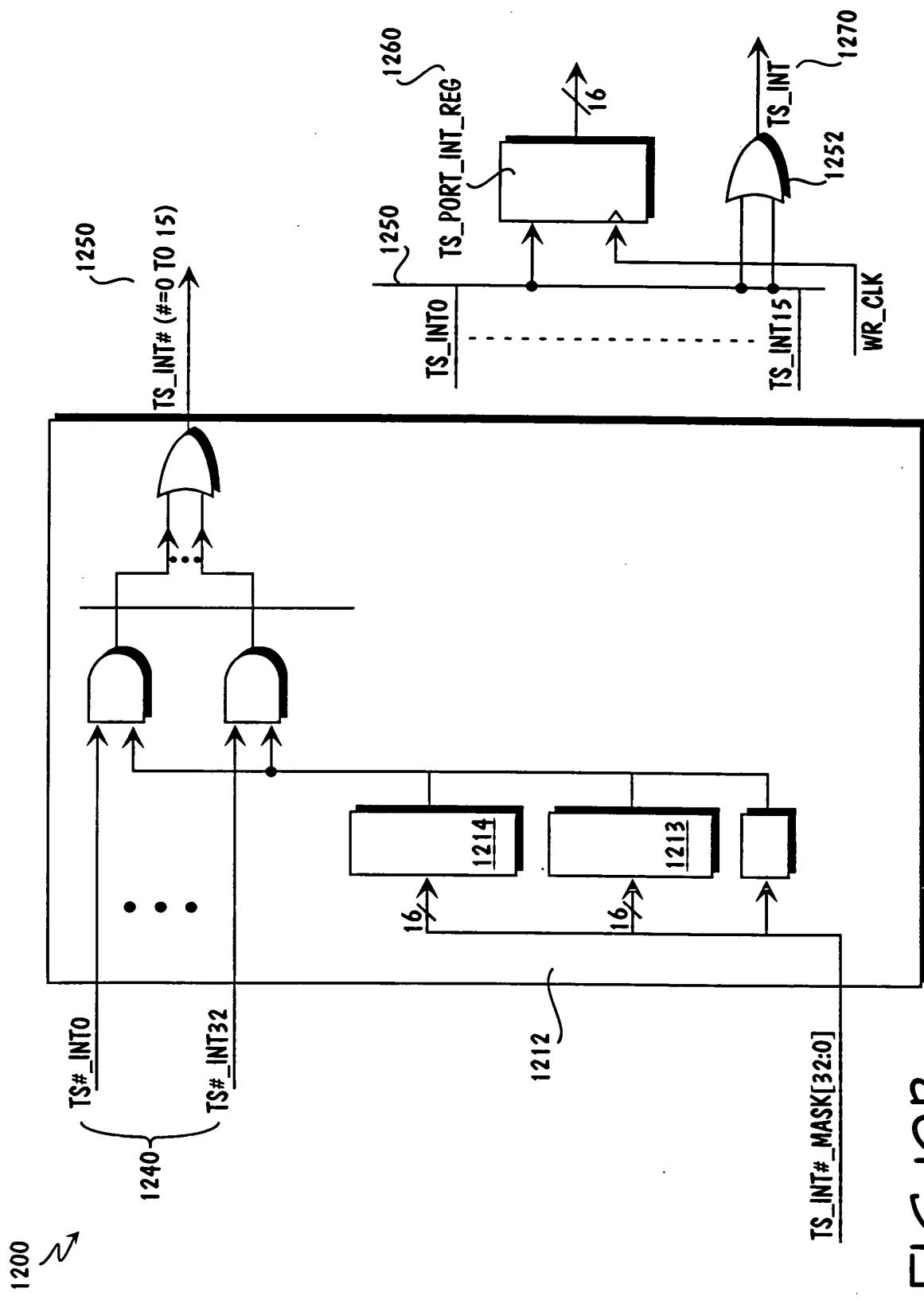


Fig. 12B

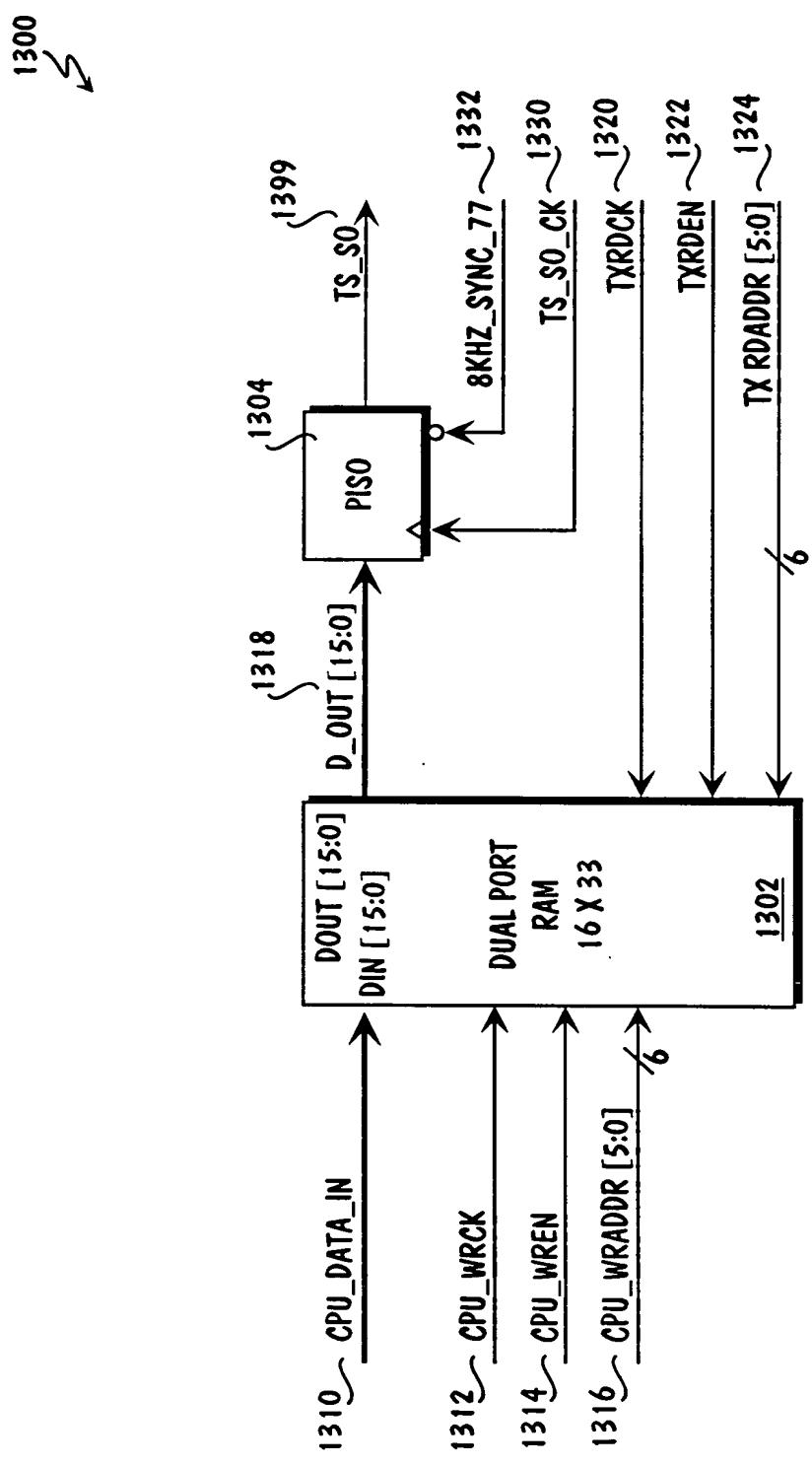


Fig. 13

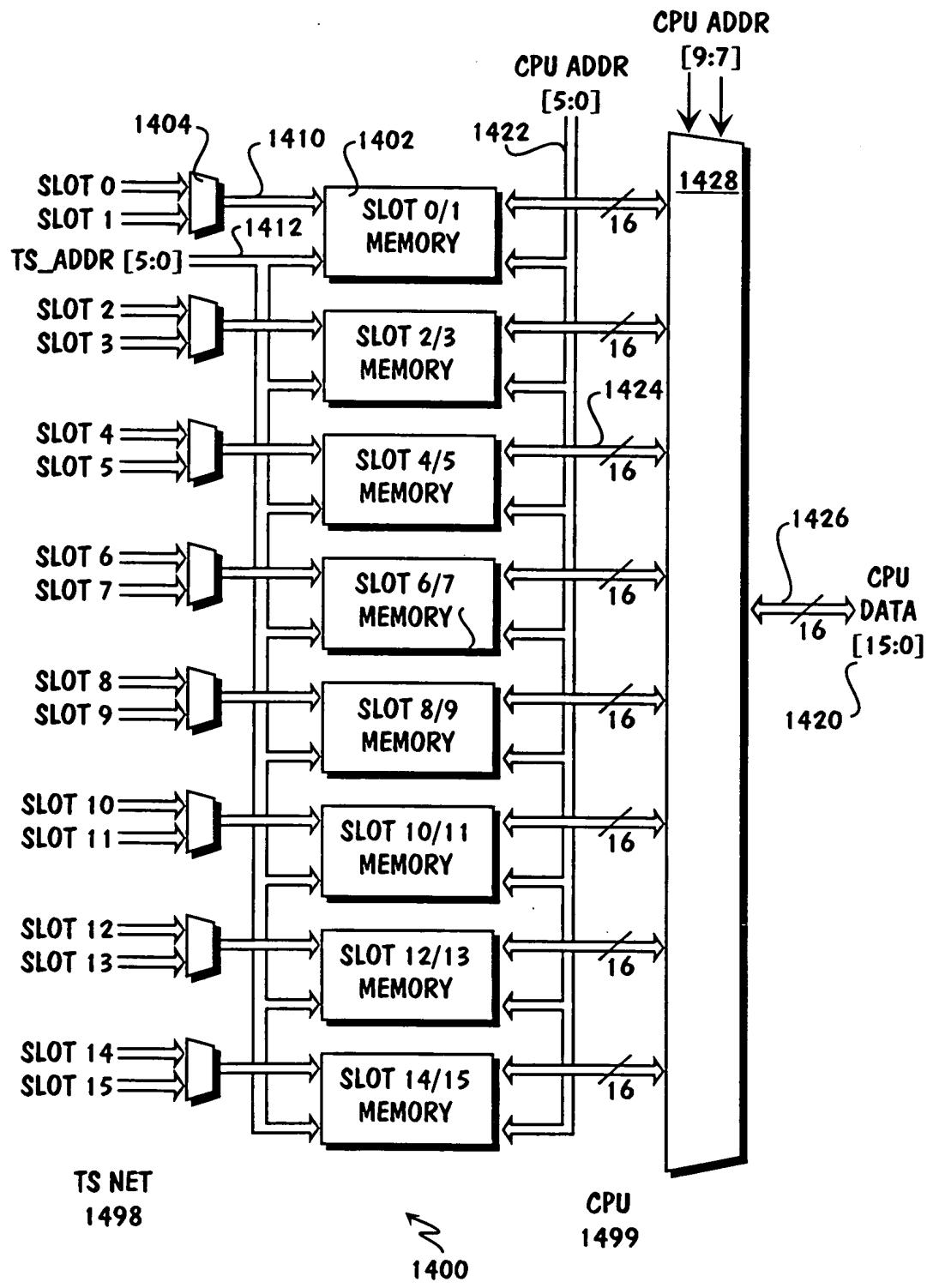


FIG. 14

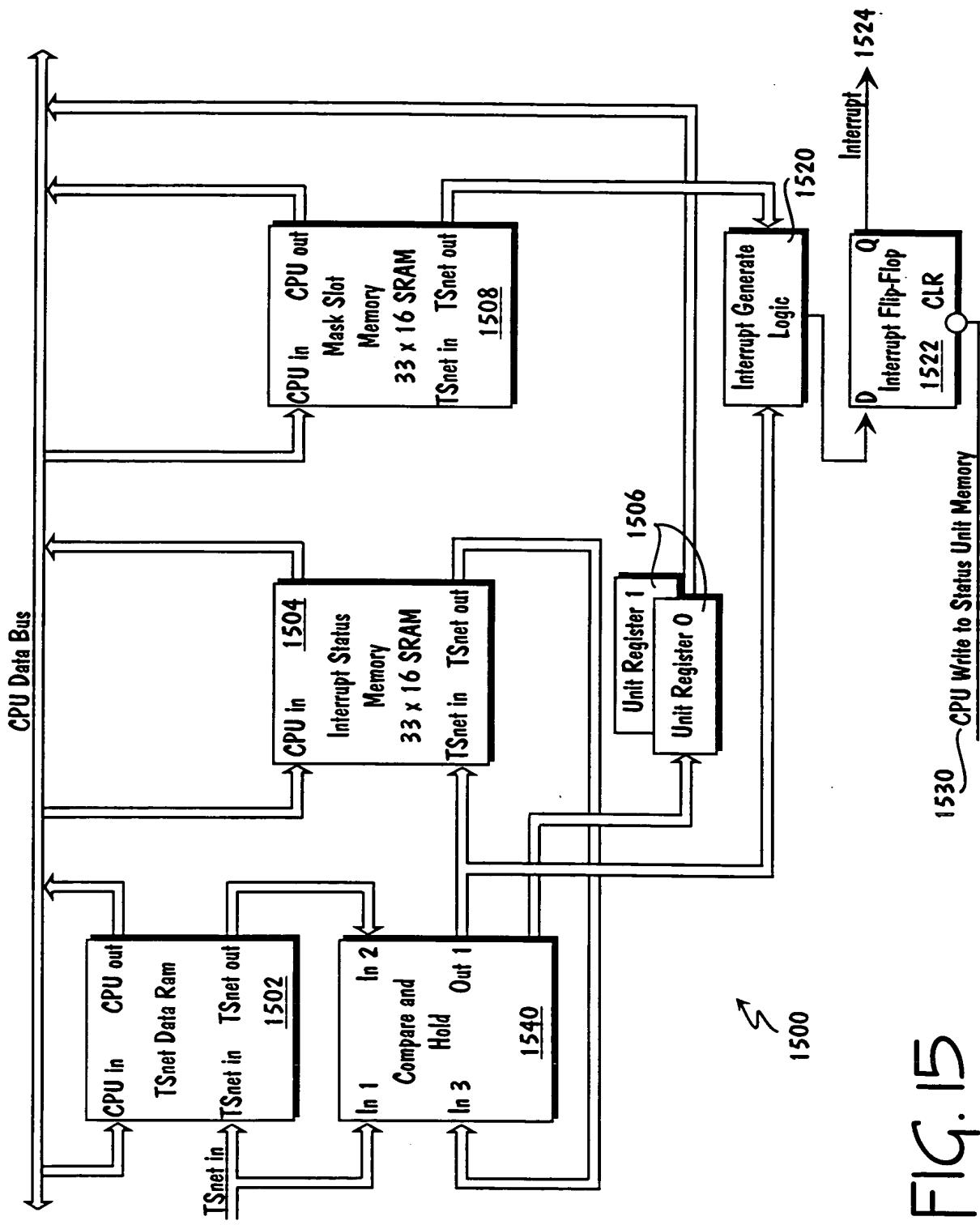
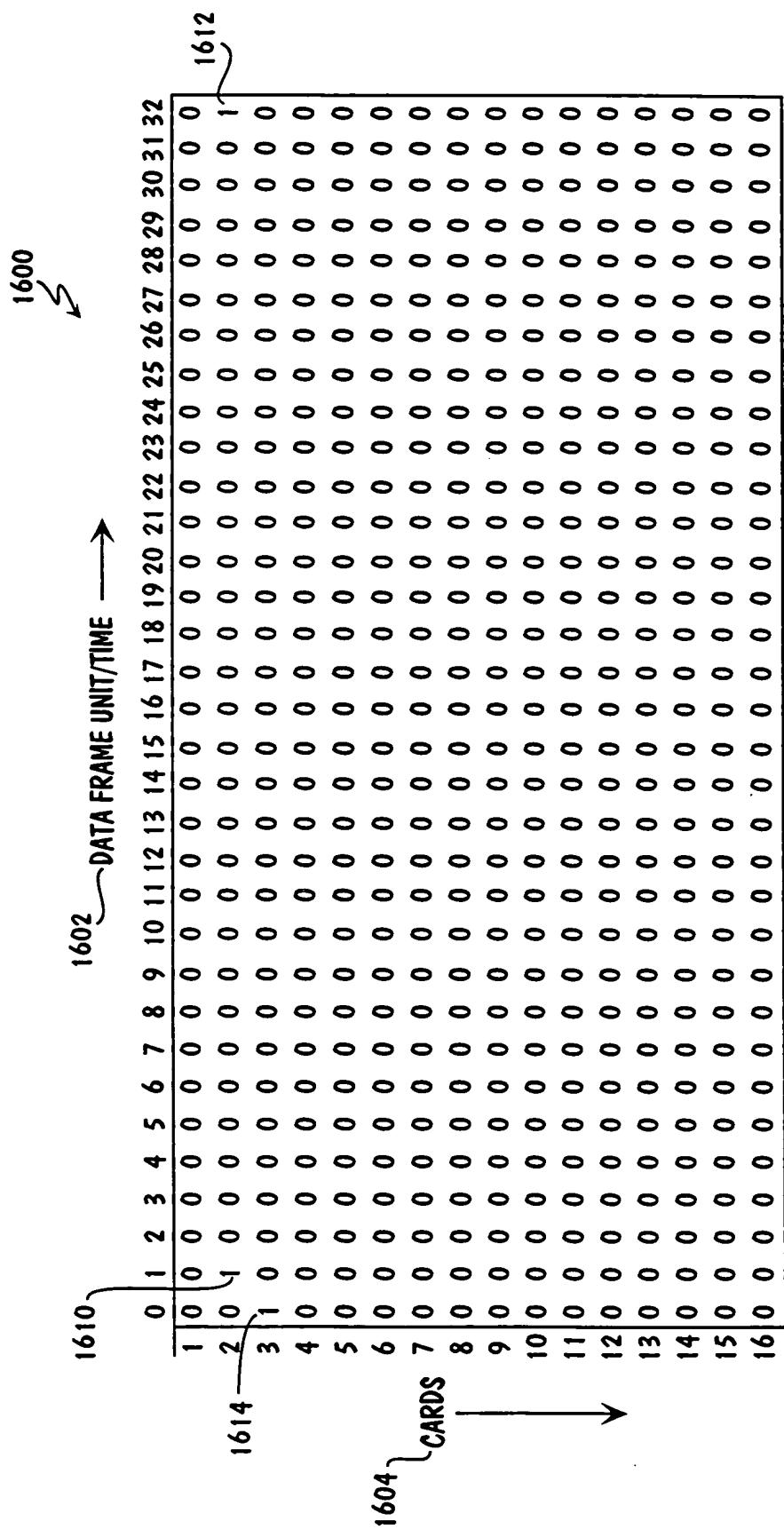


FIG. 15

FIG. 16



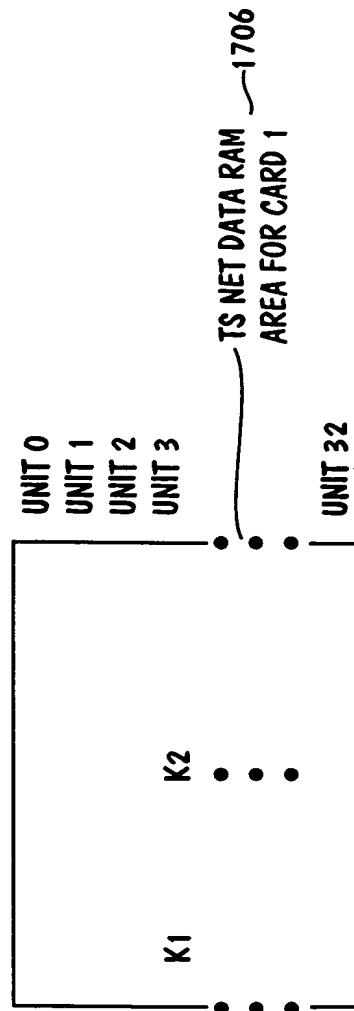
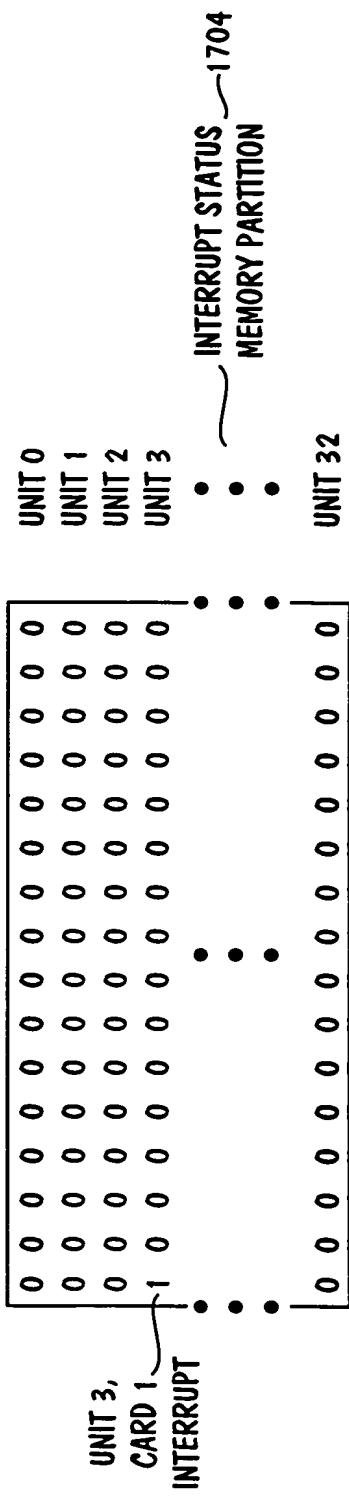
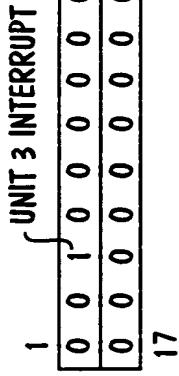
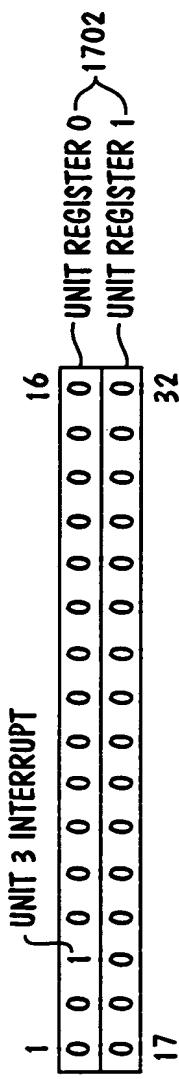


FIG. 17

FIG. 18

DATA • • • [BYTE 63] 0xFF 0xFF STATUS 0xFF BYTE 0 BYTE 1 • • •

8 KHZ FRAME _____

1800
↙

BIT	7 (MSB)	6	5	4	3	2	1	0 (LSB)
FUNCTION	BRDSTS1	BRDSTS0						
		1	1	1	1	1	1	1

STS _{B1}	STS _{B0}	INTERPRETATION
0	0	PRESNT & FAILED (OR NOT BOOTTED)
0	1	PRESNT & INACTIVE
1	0	PRESNT & ACTIVE
1	1	NOT PRESNT

FIG. 19

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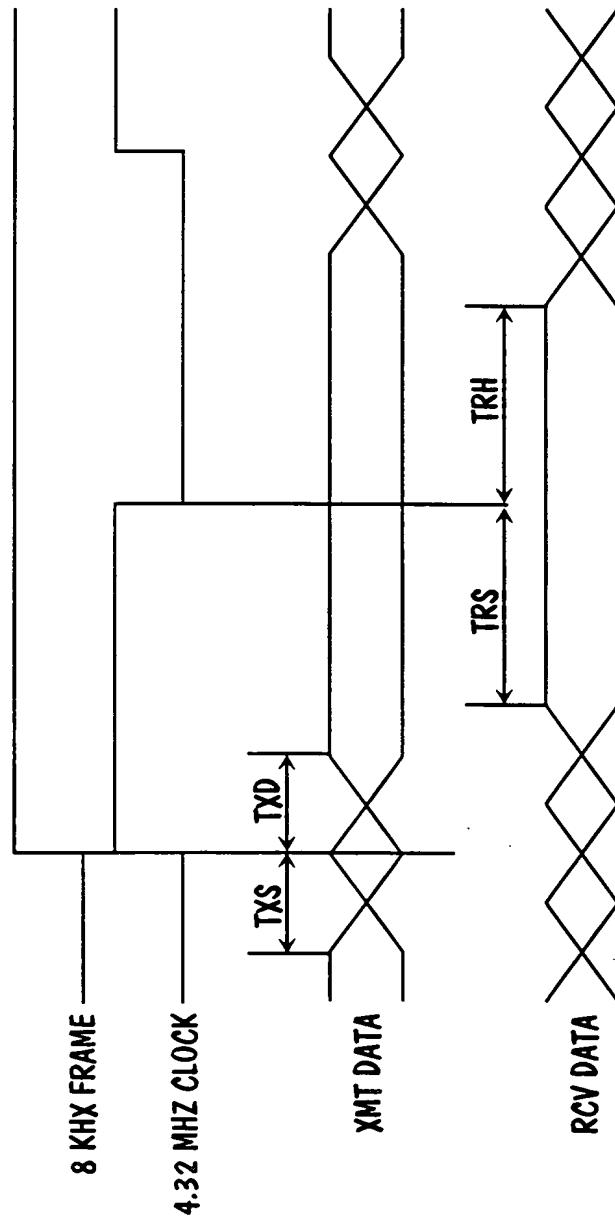


FIG. 20

FIG. 21

PARAMETER	DESCRIPTION	MIN	MAX
TXS	TRANSMIT SKEW		30 NSEC
TXD	TRANSMIT DELAY		60 NSEC
TRS	RECEIVE SETUP	30 NSEC	
TRH	RECEIVE HOLD	60 NSEC	

BYTE	POS.	POS.	POS.
0	K1 PORT 1	1	K2 PORT 2
4	K1 PORT 3	5	K2 PORT 4
8	K1 PORT 5	9	K2 PORT 6
12	K1 PORT 7	13	K2 PORT 8
16	K1 PORT 9	17	K2 PORT 10
20	K1 PORT 11	21	K2 PORT 11
24	K1 PORT 13	25	K2 PORT 13
28	K1 PORT 15	29	K2 PORT 15
32	E1 PORT 1	33	F1 PORT 1
36	SPARE	37	SPARE
40	SPARE	41	SPARE
44	SPARE	45	SPARE
48	SPARE	49	SPARE
52	SPARE	53	SPARE
56	SPARE	57	SPARE
60	SPARE	61	SPARE

FIG. 22

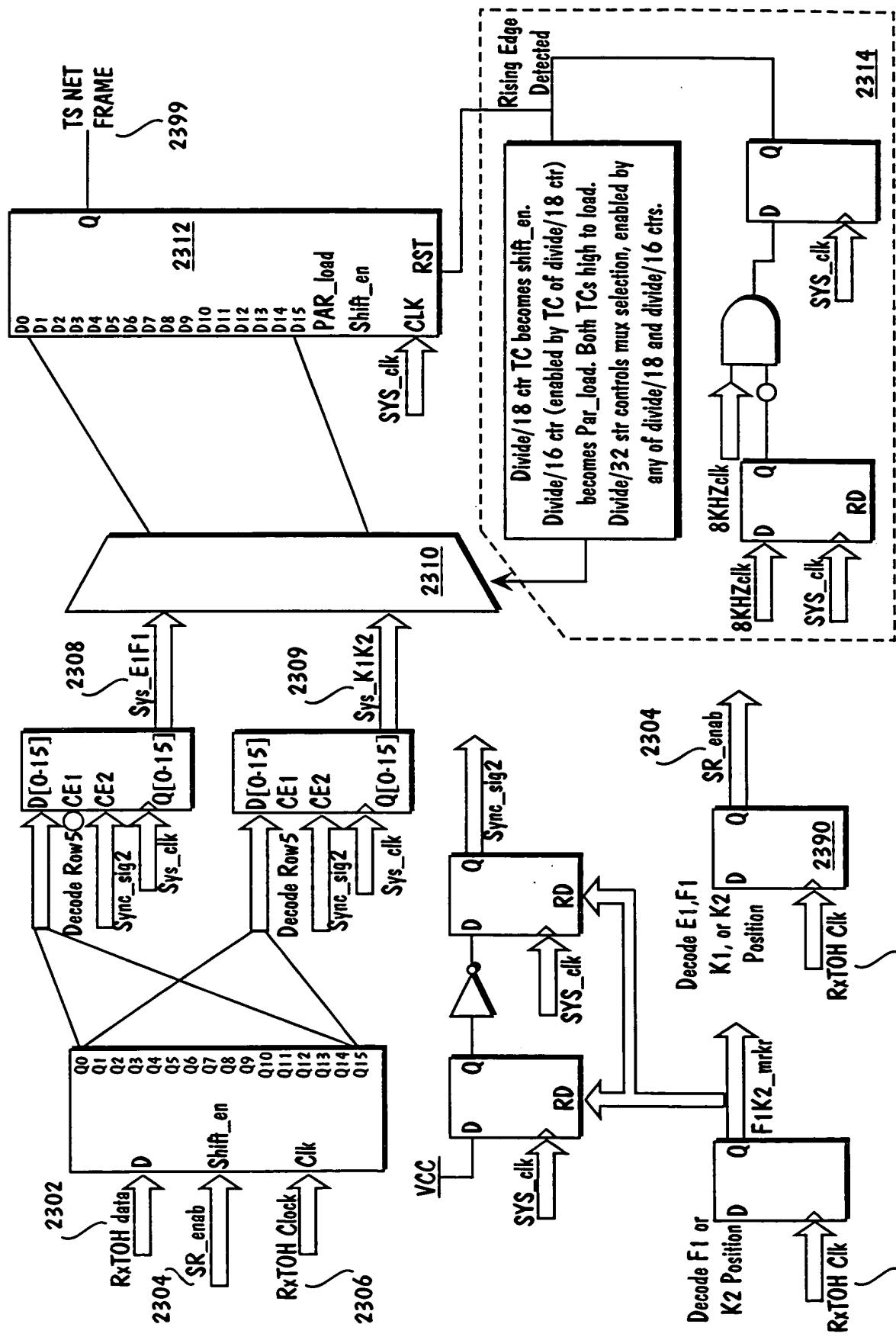


FIG. 23

2300

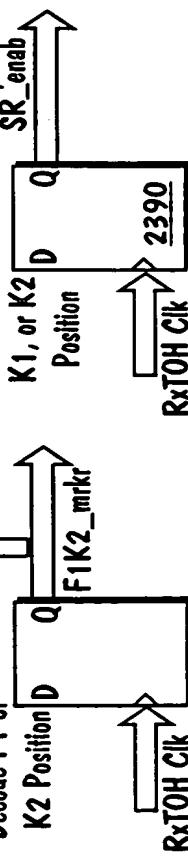
2306

2304

2314

Rising Edge Detected

Divide/18 ctr TC becomes shift_en.
Divide/16 ctr (enabled by TC of divide/18 ctr)
becomes Par_load. Both TCs high to load.
Divide/32 str controls mux selection, enabled by
any of divide/18 and divide/16 ctrs.



2304

2390

RxTOH Clk

RxTOH Clk

2306

2306

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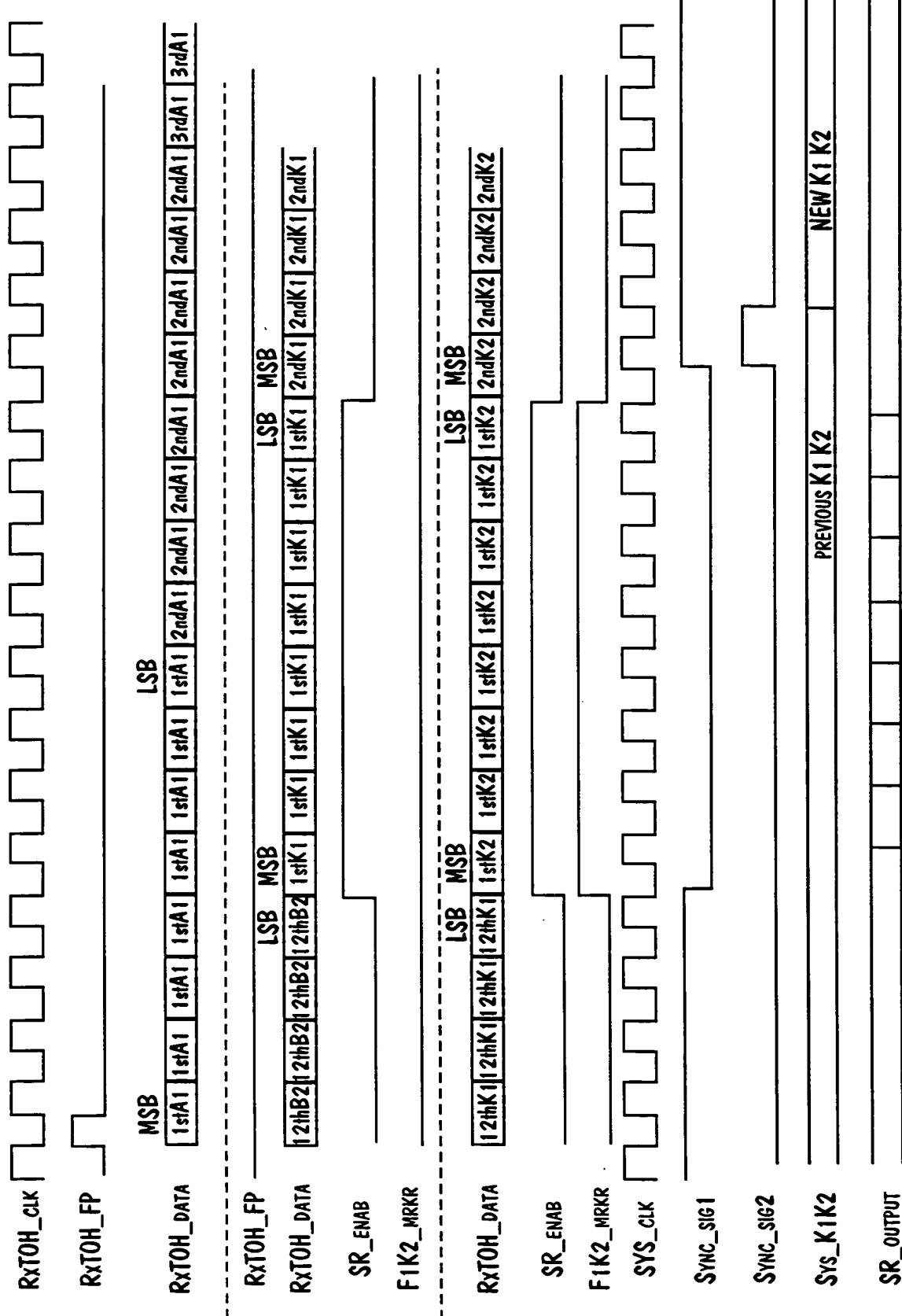


FIG. 24

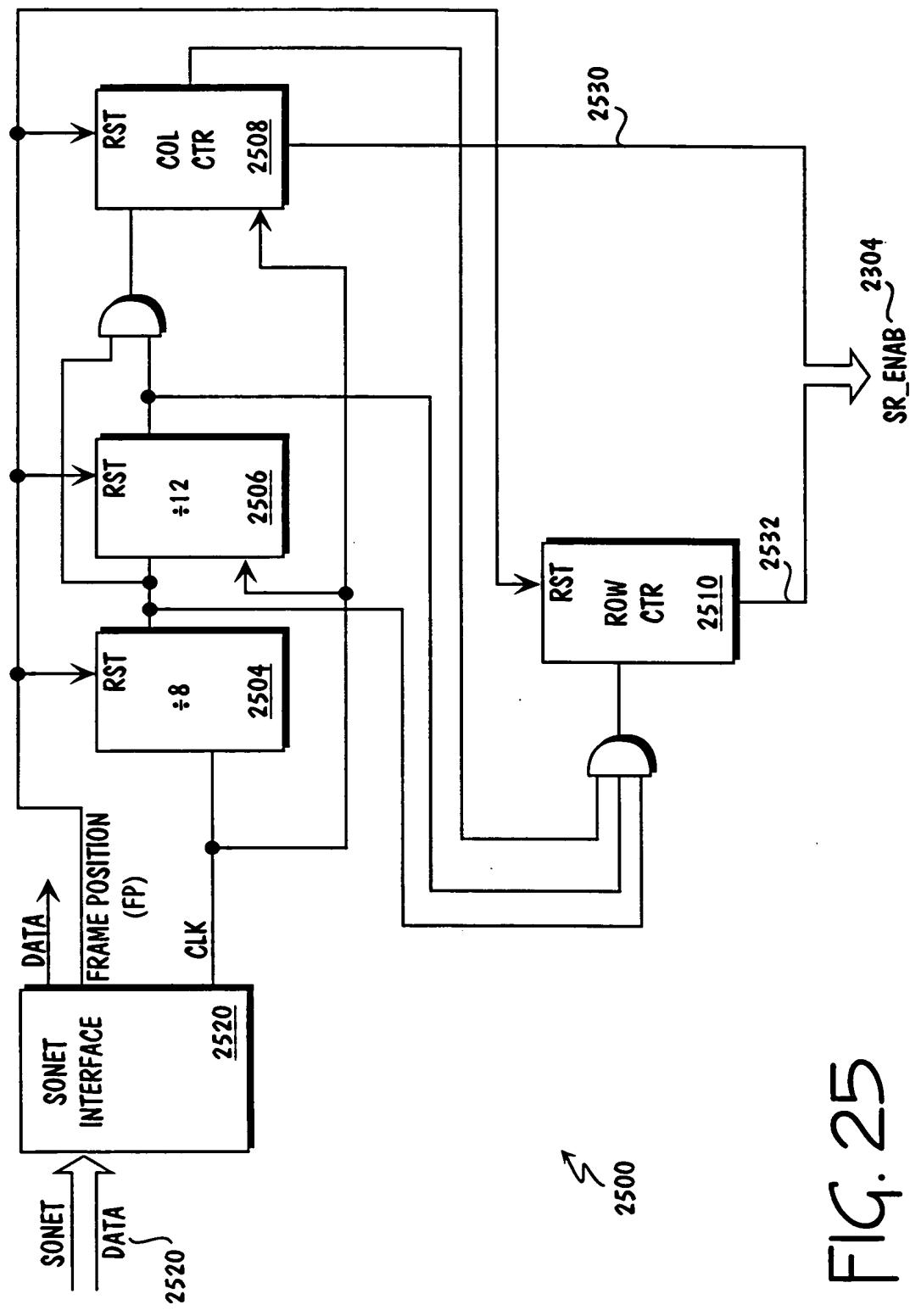


FIG. 25

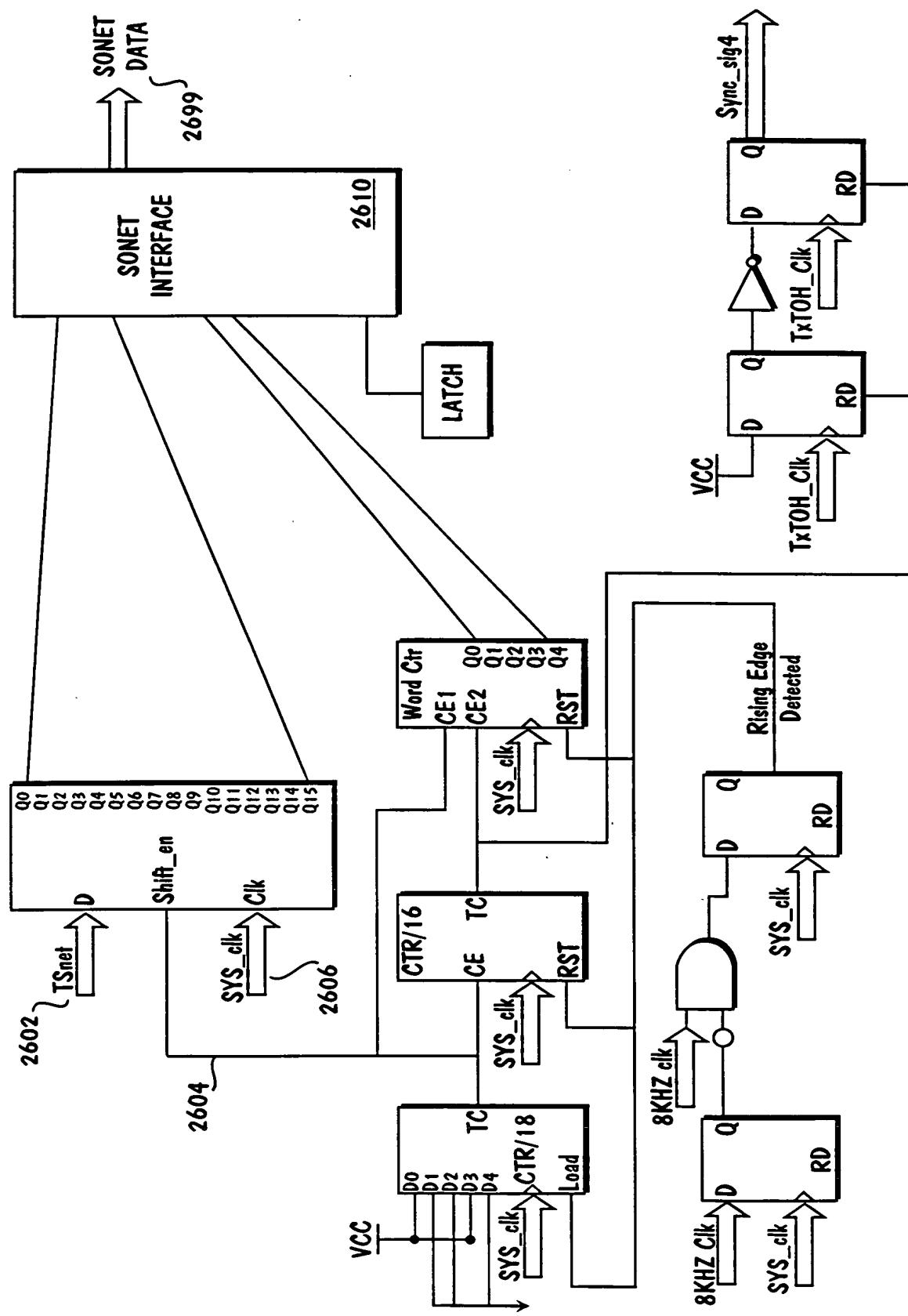


FIG. 26

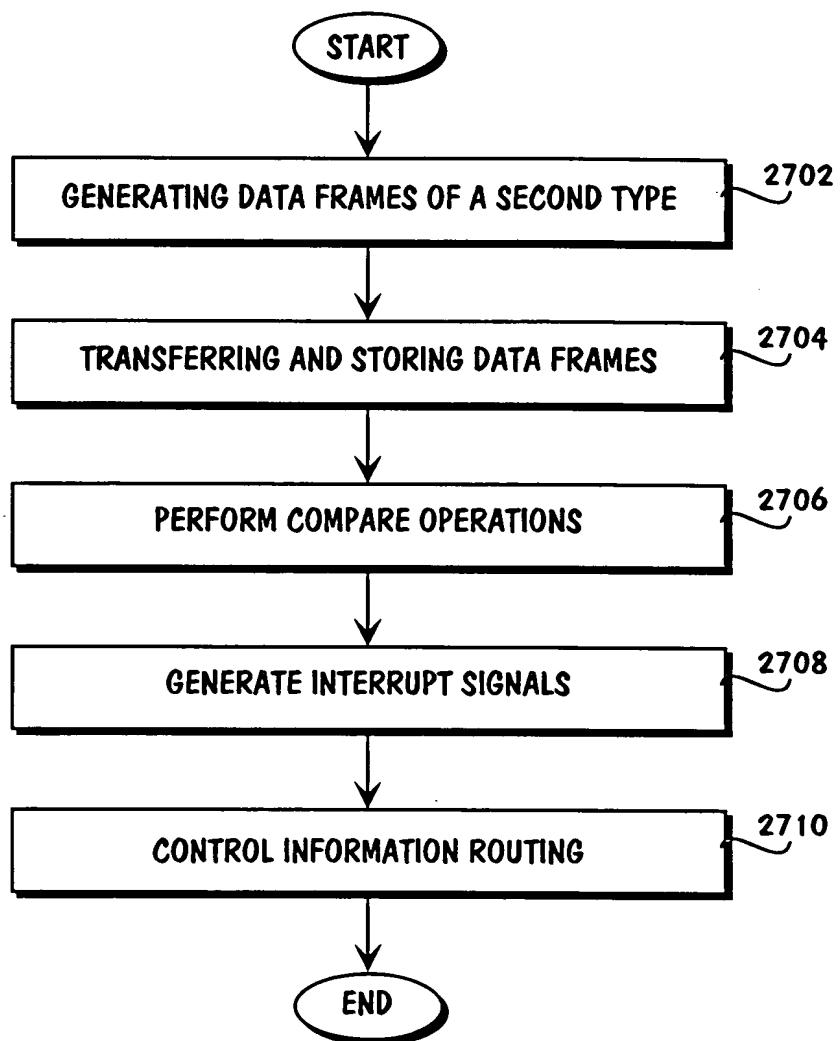


FIG. 27

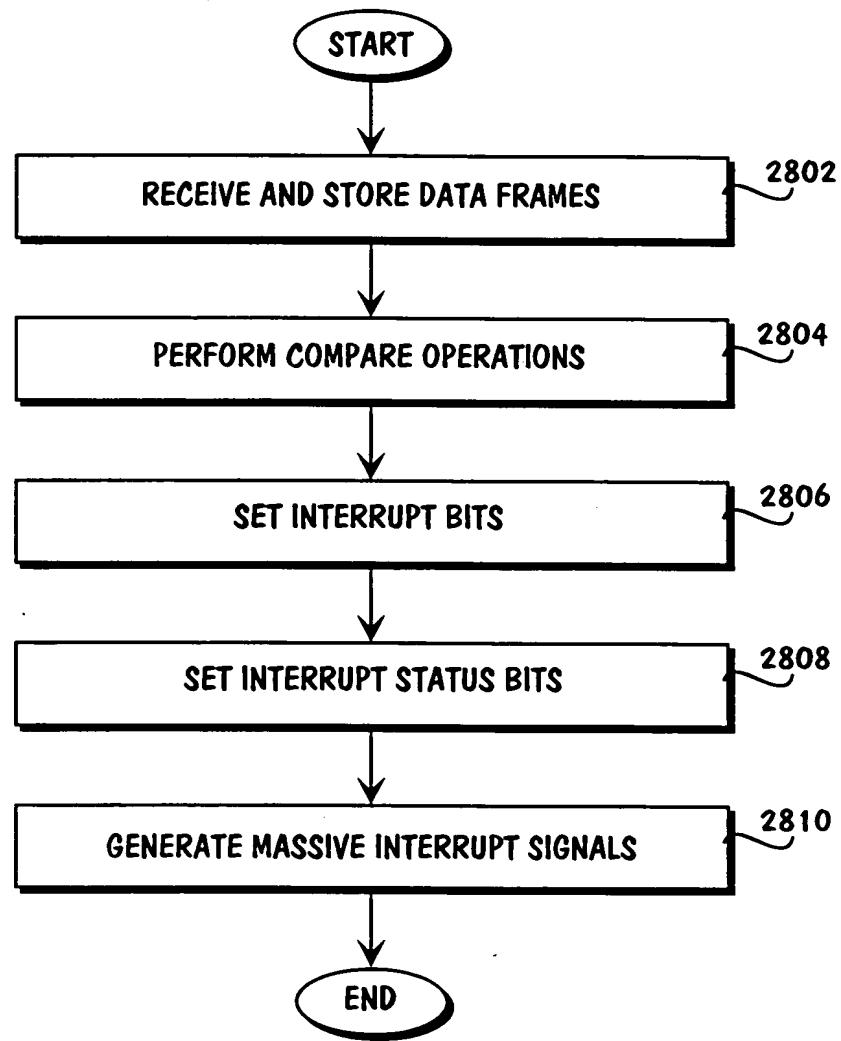


FIG. 28

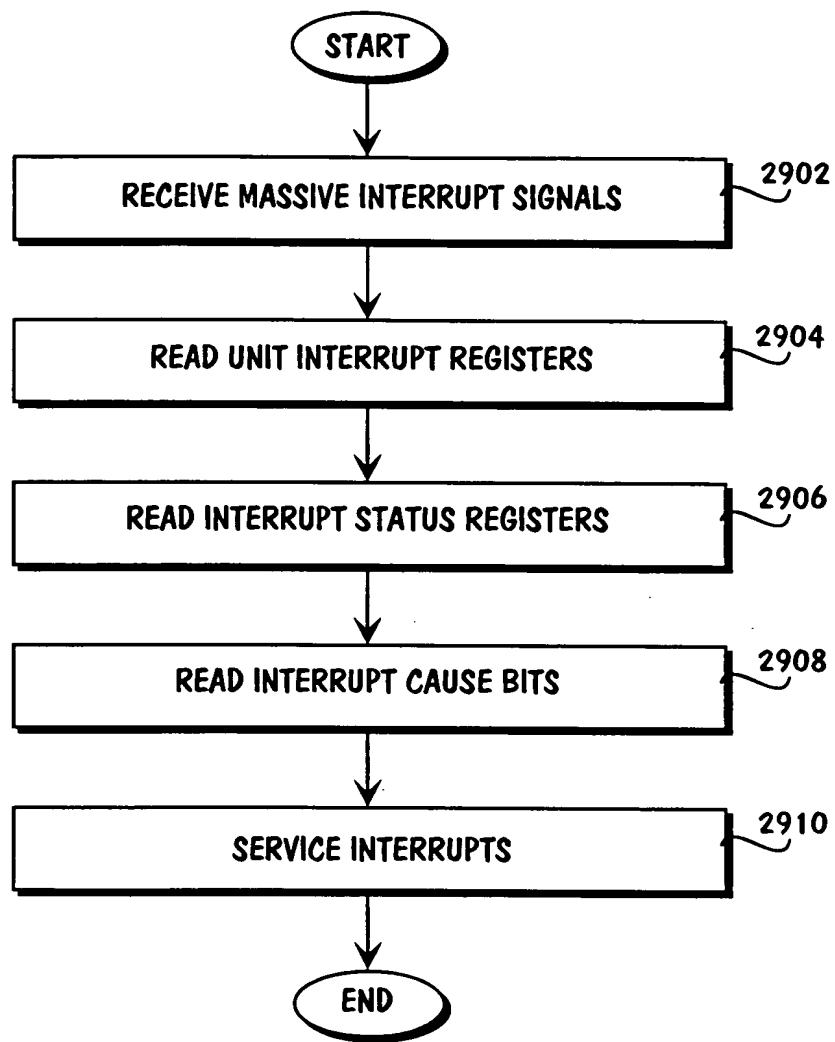


FIG. 29